

THE SNS LINAC RF CONTROL SYSTEM*

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Abstract

The SNS linac RF control system (RFCS) is currently in development. A system is being installed in a superconducting test stand at Jefferson Laboratory presently. Two systems will soon be installed at Oak Ridge National Laboratory (ORNL) and more are due to be installed early next year. The RF control system provides field control for the entire SNS linac, including an RFQ and 6 DTL cavities at 402.5 MHz as well as three different types of cavities at of 805 MHz: 4 CCL cavities, 36 medium beta superconducting (SRF) cavities, and 45 high beta superconducting cavities. In addition to field control, it provides cavity resonance control, and incorporates high power protect functions. This paper will discuss the RFCS design to date, with emphasis on the challenges of providing a universal digital system for use on each of the individual cavity types. The RF control system hardware has been designed to minimize the amount of changes for all of the applications. Through software/ firmware modification and changing a couple of frequency-dependent filters, the same control system design can be used for all five cavity types. The SNS is the first to utilize SRF cavities for a pulsed high-current proton accelerator, thereby making RF control especially challenging.

1 SYSTEM IMPLEMENTATION

Figure 1 shows a block diagram of a typical RFCS. The dotted lines represent different VXibus modules that perform the functions described above. The overall design of the SNS relies on a variety of cavity types as well as RF sources [1]. Due to physical layout constraints, a single VXibus crates houses a single RFCS for the RFQ, and each DTL and CCL cavity. However, we take advantage of the smaller klystrons and power supply configuration for the SRF sections to increase the number of systems in each crate. For the medium-beta sections, there are typically three RF control systems housed in a single crate, while for the high-beta, two systems per crate are the norm. The VXibus architecture takes advantage of the backplane in order to stream-line data-acquisition, system-monitoring and real-time-event-processing tasks. The VXibus serves as an interface for the global experimental physics and industrial control system (EPICS) to send and receive information about the way the RFCS controls the in-phase and quadrature (I/Q), rather than amplitude and phase, components of the accelerator cavity RF field.

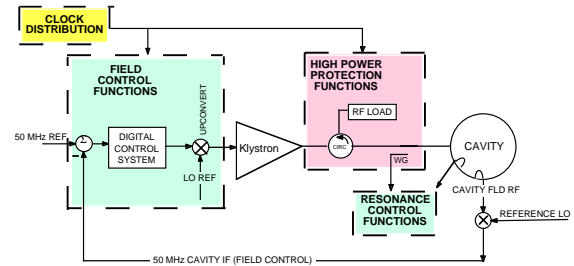


Fig. 1. RFCS block diagram, module function emphasis.

2 DIGITAL TECHNOLOGY EMPHASIS

The core module of the system that perform the field and resonance control functions (FRCM) uses digital feedback- and feedforward-controls to regulate the field parameters of an RF cavity of the SNS linac. The FRCM relies on Complex Programmable Logic Devices (CPLDs) and two digital signal processors optimized for real-time signal processing. The FRCM performs feedback- and feedforward-control algorithms on the field intermediate frequency (IF), resulting in baseband-control in-phase and quadrature (I/Q) outputs, which are then upconverted to the appropriate carrier frequency prior to amplification by the klystron.

The initial input signals are RF or IF signals that are digitized and processed. For the Field and Resonance Control Module (FRCM), the I/Q demodulation consists of sampling the 50 MHz IF signals with a 40 MHz clock, in order to produce quadrature I, Q, -I, -Q samples. These are then properly multiplexed and then filtered. Once filtered, they are compared to set-point tables and control algorithms are performed.

The control algorithms are implemented by a hybrid CPLD/DSP-based architecture in which the fast critical path signal is processed with CPLD technology for fastest throughput and minimum latency. The feedforward and resonance-control algorithms are processed through the DSPs to take full advantage of the computational power of their advanced DSP technologies. The signal-flow diagram is shown in Figure 2. The colors indicate the flow between the individual DSPs and the channels they interact with.

It should be noted that a Global Controls (EPICS) interface allows the operator to set up the RFCS in a variety of ways. Registers on the module provide access to all manners of control – set points, thresholds, mode selection, controller type, etc.

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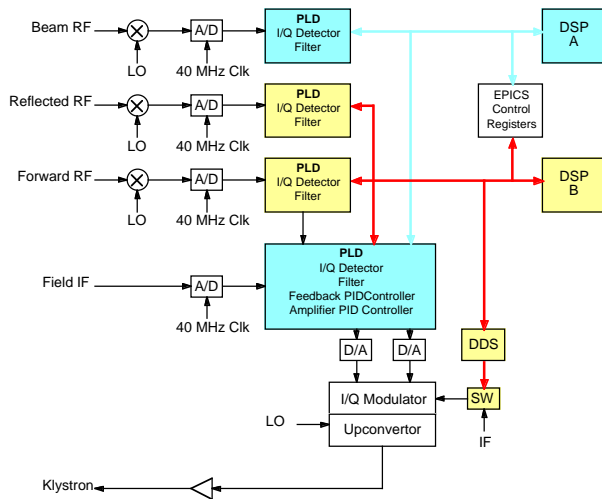


Figure 2. Signal flow of the FRCM

The FRCM uses a motherboard/daughterboard hardware architecture with three plug-inboard slots, two for the DSP boards and one for the front-end RF boards. The motherboard provides the interfaces to the RF and DSP modules, along with signal processing and diagnostic functions. The two daughter board-based Texas Instruments TMS320C6203B digital signal processors (DSPs) provide the intelligence for controlling most of the functions of the FRCM, including the digital beam feedforward loop, resonance control and monitoring, fault monitoring, supervisory control of the analog functionality, and the VXIbus-interface function.

The fault-response function of the FRCM consists of turning off the RF power in response to an external fault and initiating a fault if the PID controller saturates, a quench is detected (for superconducting cavities only), or the FRCM built-in test (BIT) logic detects a module fault. The BIT error's fault responses are programmable through EPICS and DSP interfaces. The control of the FRCM is accomplished through the shared-memory A24 VXIbus interface with EPICS. The control parameters are set through the EPICS interface, and the DSPs provide the direct interface to the control register and hardware.

3 DSP DATA FLOW

The cavity field error of each RF pulse period is stored in dual-port RAM on the motherboard. This data needs to be transferred to the DSP internal data RAM due to the two DSP architecture of the FRCM. Both DSPs share the same address bus and data bus; therefore, there may be conflicts when both DSPs have access to the data bus because data that is requested by one DSP may be retrieved to the other DSP. Hence, the cavity-field-error data in dual-port RAM must be transferred to the internal RAM via direct memory access (DMA). Full-size data is not needed for diagnosis (in the case of the 20-MHz and 1.1-msec RF ON period, 22000 samples of each signal will suffice). Instead, decimated data is to be transferred to the VXI dual-port RAM. This decimation and massive data transfer requires DMA. Much of our DSP code

development (done in C) has been based on the DMA that must occur for all computations. We have used MATLAB/Simulink models in order to develop the actual algorithms themselves [2].

4 SAME HARDWARE, DIFFERENT FIRMWARE

It should be noted that another of the RF Control System modules, the High Power RF Protect Module (HPM), utilizes a PLD as well. The HPM has many operator settable thresholds and trip points. Using a PLD to incorporate these into a single logic chip clearly saves real estate on the board, as well as provides the designer with an easy way to modify the logic as operational experience is gained, and requirements change.

The SNS utilizes five different cavity types in its linac. There are three normal conducting cavity types: an RFQ, 6 DTLs and 4 CCL. Superconducting cavities include 36 medium beta superconducting (SRF) cavities, and 45 high beta superconducting cavities. The RF Control system has specific requirements for the linac as a whole: cavity field control within $\pm 0.5\%$, $\pm 0.5^\circ$, resonance control of each cavity, as well as protecting the high power hardware (klystron and transport lines). There are also a number of system-level operational requirements such as interfacing through EPICS, and being part of the Machine Protect System (MPS, a system which is the hardware protection of the accelerator due to hardware failures anywhere along the machine.). Through use of this digital technology foundation, we have developed hardware which allows us to modify the application of each system simply by changing operator-defined parameters, or by implementing different software algorithms. The required functions and the differences between the normal conducting and superconducting portions are delineated in Table 1. Briefly it is explained by the following (red indicates the system requirement): The subheadings under Field Control Resonance Control and High Power Protect refer to specific conditions under which we need to perform those functions. For instance we need to maintain the cavity field in the presence of the beam, klystron power supply ripple, Lorentz Force Detuning (SRF cavities only), etc. Depending on the cavity type, we simply download new values into the cavity loop gains and feedforward constants in order to operate a different cavity. We do perform a pre-detune of the cavity tuner in order to offset Lorentz Force Detuning effects.

Resonance control takes place for all cavity types.

Because the normal conducting cavities have relatively broad Q curves, we can rather easily determine their resonance frequency and monitor the cavity admittance which enables us to drive a tuning device (cavity cooling water control system). However, due to the high Q of the superconducting cavities we must first do a coarse frequency sweep and then fine-tune the tuner position before declaring the cavity on resonance and ready for beam. In either case, though, we use the same hardware

and just implement different algorithms to drive the tuning mechanisms.

Table 1: Required RF Control System functions: NC versus SRF cavity systems

Required Function	NC	SRF	NC/SRF Differences
Field Control			$\pm 0.5\%$, $\pm 0.5^\circ$ ($\pm 0.75\%$, $\pm 0.75^\circ$ disables beam)
Beam loading	X	X	cavity loop gains, feedforward constants
Beam noise	X	X	cavity loop gains, feedforward constants
Klystron Performance	X	X	amplifier loop gains
Microphonics		X	cavity loop gains
Lorentz Force Detuning		X	cavity loop and feedforward, tuner preset
Resonance Control			frequency range cavity-type specific
1st Determine Res. f	X	X	sweep, find, tune (NC-water, SRF-motor)
Setup Coarse	X	X	NC - calc. admittance; SRF - freq. sweep
Fine tune (w/in Hz)		X	cavity phase ring down measurement
Provide Tuner info.	X	X	same method - error
HPRF Protection			# of monitors differs per cavity type
High Reflected Power	X	X	none
Waveguide Arc (f/o)	X	X	none
Cavity Arc	X	X	same algorithm in HPM
Cavity Quench		X	algorithm in FRCM
Interact with EPICS	X	X	# of channels differs per cavity type
Interact with MPS	X	X	none
Interact w/ Timing Sys.	X	X	none
Provide RF Reference	X	X	none
Cavity Calibration		X	signals available from FRCM

Through our MATLAB/Simulink system modeling we have defined the setpoint tables necessary to achieve the correct power levels in each cavity, no matter the cavity's bandwidth. Similarly Simulink is used to provide initial feedforward tables for each operating mode and cavity type [3].

5 DRAWBACK OF NEW HARDWARE

Designers should be aware of a potential drawback associated with any system that utilizes "state of the art" technology. There is a risk associated with using the latest version of a new chip design. We found that for one version of a particular chip, we needed one version of the programming software. But when we later upgraded with the newer version "pin for pin compatible" part, the software we were using would no longer program the chip properly. In addition, in one instance we designed the printed circuit card as recommended, but when we tested it, we had trouble. As a direct result of our consultation with the manufacturer, a later errata application note was issued. In essence, we turned out to be a "beta" site for two different components. This is a difficult position to be in and can lead to hours of frustration in the lab.

6 SUMMARY

Digital technology has allowed us to greatly reduce the amount of space taken up by an RFCS, while at the same time increase the number of functions it performs. Fifteen years ago one analog RFCS filled a 19" equipment rack. Ten years ago we shrunk it to 3/4 of a rack, and then to

half a rack. The majority of the hardware was still analog with one digital-based module. Five years ago, only a quarter of a rack (one full VXI crate) was required, with an even split between digital and analog circuitry. Today the primarily digital system layout is limited more by the HPRF layout than anything else. For the systems which require large, high power klystrons we only have one RFCS in a half empty VXI crate. For the SRF cavities which have much smaller klystrons, and share a convertor/modulator, and are therefore all in close proximity of each other, we have 3 RFCS in one VXI crate for the medium beta cavities, and 2 per crate for the high beta section.

In conclusion, we have been able to use the same digital hardware for different cavity types, and rely on software/firmware to provide the necessary RF Control System functions and to meet the requirements set forth by the accelerator designers.

7 REFERENCES

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